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Vertical Conductive Structure Technology: Simulation and Measurement

Chaofeng Li, Missouri University of Science and Technology
[clf83@mst.edu]

Junyong Park, Missouri University of Science and Technology
[junyongpark@mst.edu]

Aritharan (Hari) Thurairajaratnam, Microsoft
[harit@microsoft.com]

Eddie Mok, Wus Printed Circuit Kunshan Co. Ltd
[eddie_mok@wustec.com]

Joe Dickson, Wus Printed Circuit Kunshan Co. Ltd
[1144@joedwuspcbintl.com]

Joan Tourné, NextGin Technology
[j.tourne@nextgin-tech.com]

DongHyun Kim, Missouri University of Science and Technology
[dkim@mst.edu]

Abstract

Vertical conductive structure (VeCS) technology, an advanced interconnect technology for signal transition on different printed circuit board (PCB) layers, was developed to meet needs for more intelligent PCB technologies with decreased layer count, and improved signal integrity and power integrity with respect to those of conventional transition via structures. In contrast to the conventional via structure, the VeCS consists of a plate signal trace and an oval-shaped shielding ground racket comprising a semi-coaxial structure or a vertical transmission line. The VeCS achieves a continuous characteristic impedance that improves electrical performance regarding losses, crosstalk, and electromagnetic interference. Herein, the physical structure of the VeCS is first introduced. Subsequently, the time domain reflectometer impedance of the VeCS is extracted and analyzed through full-wave simulations. The crosstalk between VeCS-based and via-based channels on the PCB is compared to clarify the advantages of VeCS technology. Finally, measurements are used to further demonstrate the advantages of VeCS technology.

Authors' Biographies

Chaofeng Li is a Ph.D. student in electrical engineering at Missouri University of Science and Technology (formerly University of Missouri–Rolla), Rolla, MO, USA. His current research interests include signal integrity, high-speed channel simulation and modeling, PCB and package material characterization, and on-chip PDN modeling.

Junyong Park received a B.S. degree in electronic and electrical engineering from Sungkyunkwan University, Suwon, Korea, in 2014, and M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2016 and 2019, respectively. He was a senior engineer with the DRAM design team, SK Hynix, Icheon, South Korea, from 2019 to 2023. In March 2023, he joined the Missouri University of Science and Technology (formerly University of Missouri–Rolla), Rolla, MO, USA, where he is currently a postdoctoral fellow. His research interests include statistical signal/power integrity in high-speed systems, EMI/EMC, and IBIS-AMI.

Aritharan (Hari) Thurairajaratnam is a principal engineer at Microsoft with more than 25 years of experience in digital high-speed design and signal integrity. He holds multiple patents in the area of enhancing electrical performance for package substrates and PCB design. His current focus includes improving the electrical interface between large scale package devices to either network or system side topologies in the 200+ Gbps regime. Hari received B.S. and M.S. degrees in electrical engineering from the University of Arizona, Tucson, in 1994 and 1997, respectively.

Eddie Mok has been AVP at the Wus Printed Circuit Product Innovation Development group since 2006, and has worked on developing advanced CPB interconnect material,

manufacturing, and design solutions. Eddie had 18 years of experience in technical marketing of PCB materials before joining Wus. Eddie received B.S. and M.S. degrees in mechanical engineering from the University of California, Irvine.

Joe Dickson is the SVP of Wus PCB Intl. and has more than 40 years' experience in engineering senior management and supporting some of the most advanced PCB technical commercial and military production. His roles include process/product development, advanced environmental capability, and facility automation. He received two US patents and one international product patent. His credentials include an MBA in technology management, BS in business management, Six Sigma Master Black Belt Trainer, ISO 9002 auditor, DMAIC TQM and lean manufacturing. He has had previous engineering management roles at Cisco Systems, Tyco Electronics, SBC Inc., and Armstrong World Industries, and is currently with Wus PCB Intl.

Joan Tourné is the CEO of NextGin Technology. He has more than 30 years' experience in PCB design and PCB manufacturing, supported by several patents in the fields of processing, design, high speed, and optical interconnect. He started to work as a circuit board designer after moving to a position in engineering and management on an international level. He has been a speaker at various exhibitions at many international events.

DongHyun Kim is an assistant professor of electrical and computer engineering at Missouri University of Science and Technology, Rolla, MO, USA, and is a faculty member at the Center for Electromagnetic Compatibility, a National Science Foundation Industry/University Cooperative Research Center. His current research interests include nanometer-scale devices, through-silicon via technology, dielectric material characterization and signal integrity, power integrity, temperature integrity, electromagnetic compatibility, and electrostatic discharge in 2.5D/3D IC systems.

Introduction

Vertical interconnectors, more commonly known as vias, play essential roles in modern high-speed digital systems for connecting signals in multiplayer printed circuit boards (PCBs) and packages [1]. With increases in the numbers of integrated devices and the requirement for higher densities, vias have become ubiquitous in multilayer PCBs. Vias are used to route signals on different layers for different channels, which are typically discontinuous components in high-speed channels, and can lead to severe signal integrity and power integrity problems [2]. Therefore, designing vias with high electrical performance is essential to meet the required impedance, loss, and crosstalk specifications. Generally, 3D full-wave simulation software, such as HFSS and CST, is used to optimize the via transition. To efficiently and accurately predict the electrical performance of a conventional via, the mode-decomposition-based equivalent via model has recently been proposed and analyzed [3–4]. This model can be extended to differential via optimization [5]. Additionally, optimization of non-functional pad placement on signal vias according to multiple reflection theory has been proposed [6–7]. However, with the continually increasing data speed, conventional vias cannot achieve the required electrical performance for high-speed digital circuits.

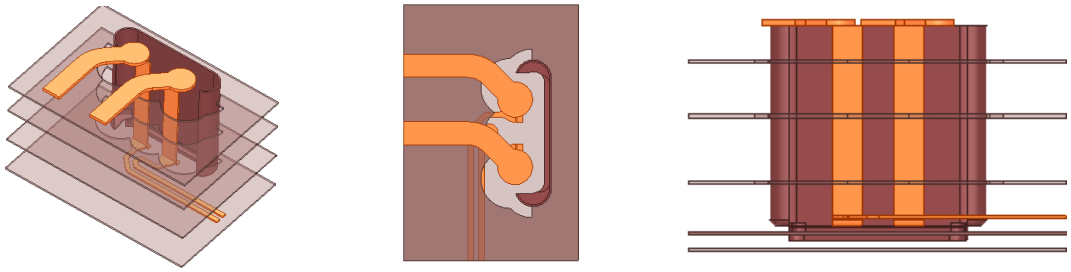
Vertical conductive structure (VeCS), a new advanced interconnect technology for signal transition on different PCB layers, was developed to meet the needs for more intelligent PCB technologies that decrease the layer count and improve the signal integrity with respect to those in conventional transition via structures [8]. A well-known issue is that the characteristic impedance of conventional vias is discontinuous, because of the changes of the reference ground plane when the via passes through the layers. Discontinuity in characteristic impedance can cause severe signal integrity problems, particularly in the high-frequency range. In contrast to the conventional via structure, the VeCS consists of a plate signal trace and an oval-shaped shielding ground racket, which is a semi-coaxial structure or a vertical transmission line. Thus, the VeCS achieves a continuous characteristic impedance that improves electrical performance regarding losses, crosstalk, and electromagnetic interference radiation. Additionally, the VeCS achieves a denser signal layout than conventional via structures for high-density interconnect applications [9].

Herein, the physical structure of the VeCS is first introduced. The fabrication procedures of the VeCS are presented and compared with those of conventional via structures. In contrast to that of the via structure, the physical structure of the VeCS is continuous, because it has a continuous reference plane, designed as an oval-shaped ground racket. The time domain reflectometer (TDR) impedance of the VeCS is extracted and analyzed through full-wave simulations. The impedance of the VeCS, in contrast to a conventional via, can be easily designed and controlled. Moreover, the crosstalk is extracted on the basis of 3D full-wave simulation for the VeCS-based and via-based channels on a PCB, and compared to clarify the advantage of VeCS over conventional via technology. Because the VeCS has an oval-shaped ground racket, the crosstalk between adjacent channels can be controlled to a very low level. The far-end crosstalk on the VeCS-based channels can be significantly less than that on via-based channels with the same signal transition density.

To further clarify the advantages of VeCS technology, we designed several fixtures and performed measurements.

Vertical Conductive Structure Technology (VeCS)

The VeCS is a new technology developed by NextGin Technology to meet needs for a more intelligent PCB technology with decreased layer counts and improved signal integrity, without a need for costly sequential technologies such as AnyLayer and modified semi-additive process technologies [8]. VeCS technology can provide a cost-effective alternative for complex fan-out from fine-pitch grid array components. Compared with the conventional via structure, the VeCS can achieve a higher density of vertical connections without requiring many stages of sequential build-up. Moreover, the electrical performance of vertical connections can be improved with VeCS technology.



(a) (b) (c)

Fig. 1. VeCS: (a) 3D view, (b) top view, (c) section view.

The VeCS consists of vertical plate signal traces and an oval-shaped racket, as shown in Fig. 1. The signal is transitioned from the top layer to the inner layer of the board through the vertical plate signal trace. The oval-shaped racket serves as the reference plate for the signal trace and can easily maintain the impedance of the signal trace to the target, as compared with conventional plated through hole (PTH) vias. Moreover, the crosstalk or electromagnetic interference from the noise source is effectively isolated by the oval-shaped racket, particularly when the noise source is located at the back side of the racket.

The VeCS is based on specially formed cavities [9]. A simple example is used to demonstrate the manufacturing process of the VeCS (Fig. 2). The fabrication process of the VeCS comprises five steps: 1, creating the principal slot; 2, plating the principal slot; 3, filling the principal slot with resin; 4, drilling the cross-route slots; 5, drilling the back-route slots; and 6, filling the cross-route and back-out slots with resin. Because the VeCS fabrication process is similar to that of conventional via structures, despite several differences, no new equipment is required for PCB manufacturing. Furthermore, VeCS technology can overcome the limitation of the conventional PTH via, because of the drilling aspect ratio. Thus, VeCS technology can achieve very high-density interconnection for future applications.

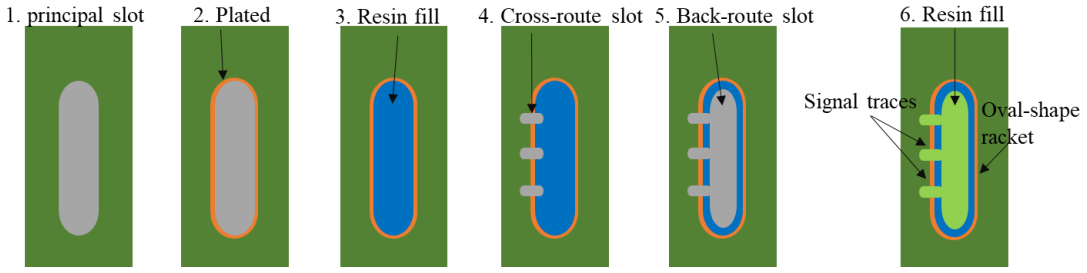


Fig. 2. The VeCS fabrication process.

Specific design rules and additional details regarding VeCS technology can be found on the NextGin technology company website [8] and prior publications [9–13].

Electrical Performance Comparison of VeCS and The Conventional Transition Via

We investigated the electrical performance of the VeCS, in terms of TDR, S-parameters, and crosstalk, through full-wave simulations and measurements.

Full-wave Simulation

To accurately evaluate the electrical performance of the VeCS, we used the full-wave simulation software (HFSS) to predict the S-parameter of a differential channel up to 70 GHz. The 3D model of the VeCS is shown in Fig. 3 (a). As described before, the VeCS consists of an oval-shaped ground racket and vertical plate signal traces. The differential micro-strip traces are located on the top layer, and the differential stripline is located on the signal layer 14 (L14) of the PCB. All the inner layers of the PCB are not depicted, to clearly demonstrate the geometry of the VeCS in Fig. 3 (a). The cross-sectional view of the VeCS is shown in Fig. 3 (b).

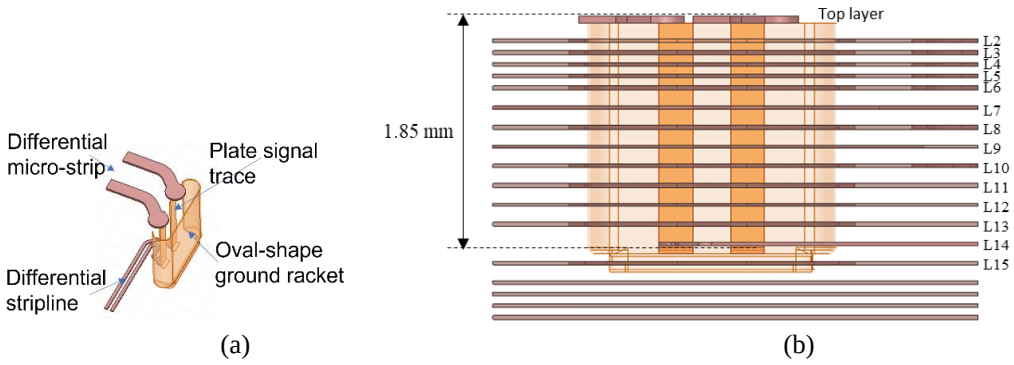


Fig. 3. The designed VeCS: (a) 3D view of VeCS without inner layers, (b) cross-sectional view of VeCS with inner layers.

The conventional differential via with same stack-up and signal trace layout as the VeCS is shown in Fig. 4 for comparison. The via pitch is 0.9 mm, and is designed for a 0.9 mm pitch ball grid array of packaging. Furthermore, the layout area for the conventional via is the same as that for the VeCS, to facilitate comparison. The Dk and Df of the board dielectric for VeCS and conventional via are 3.3 and 0.003, respectively, at 10 GHz. The Decreased and Df of the refill resin for VeCS are 4.23 and 0.003, respectively, at 10 GHz.

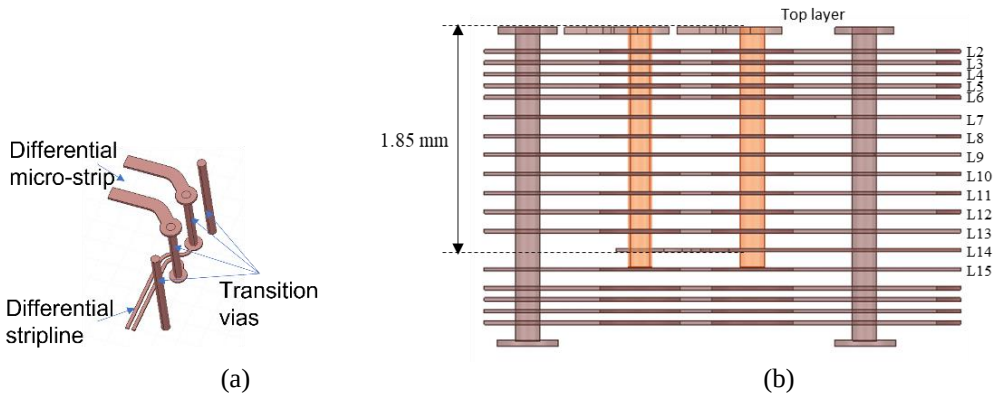


Fig. 4. The conventional differential via. (a) 3D view of the conventional differential via without inner layers. (b) Cross-sectional view of the conventional differential via with inner layers.

The S-parameters of the VeCS and the conventional differential via are plotted and compared in Fig. 5. Fig. 5 (a) shows the differential insertion loss S_{dd21}, and Fig. 5 (b) shows the differential return loss S_{dd11}. From the comparison, S_{dd21} of the VeCS is clearly less than that of the conventional via above 40 GHz. Meanwhile, the S_{dd11} of the VeCS is clearly less than that of the conventional via by at least 5 dB in the frequency 10–50 GHz.

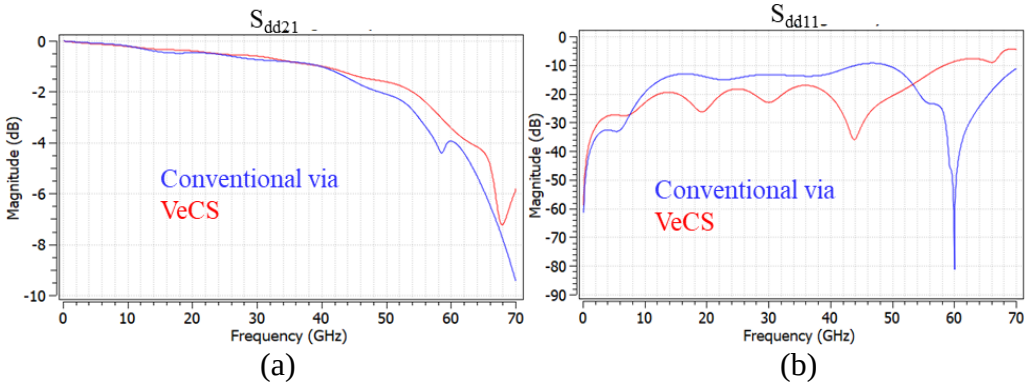


Fig. 5. S-parameters of the VeCS and conventional differential via: (a) differential insertion loss S_{dd21}, (b) differential return loss S_{dd11}.

Furthermore, the TDR impedances of the VeCS and the conventional via are compared in Fig. 6. The TDR impedance shows that the conventional via represents an inductance. The maximum impedance of the via is 114 ohms when the rise time is 15 ps. Because the via pitch is designed to be 0.9 mm for the specific pin pitch of a ball grid array. Thus the loop inductance of the via is large. However, the maximum impedance of the VeCS is 104 ohms, because of the transition structure of the microstrip to the vertical plate trace. The TDR impedance explains why Sdd21 and Sdd11 of the VeCS-based channel are less than that of the conventional via-based channel in certain frequency bands. The conventional via and the VeCS were designed as the test vehicle 1 (TV1) for preliminary comparison for crosstalk. Conventional via structures and VeCS are not optimized to the target impedance, and identical neck-down structures were used to transition to conventional via and VeCS, for fair comparison. The test vehicle 2 (TV2) set with optimized impedance for the VeCS and the conventional via comparison will be presented in the future.

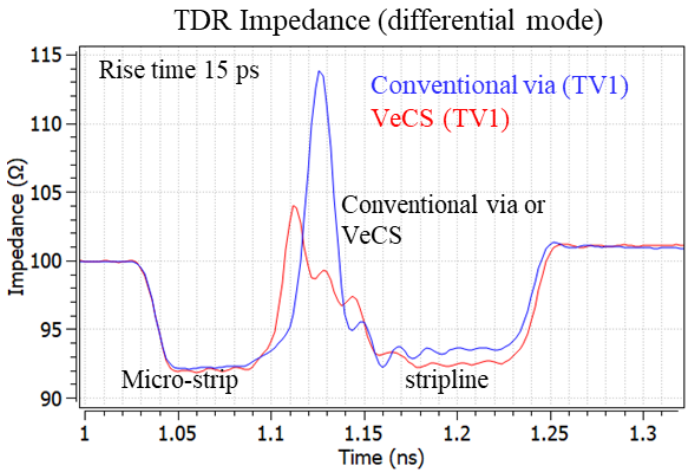
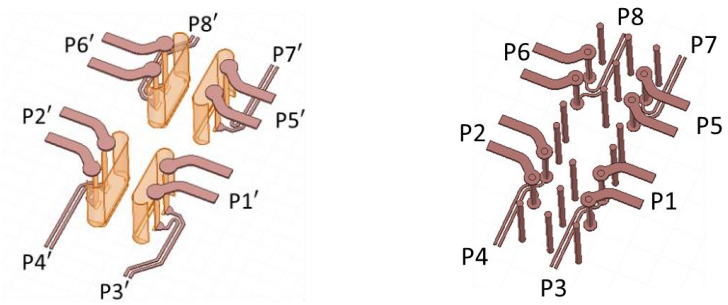


Fig. 6. Differential mode TDR impedance of VeCS and conventional via. (The first peak of VeCS TDR impedance comes from the transition structure of Microstrip to VeCS.)

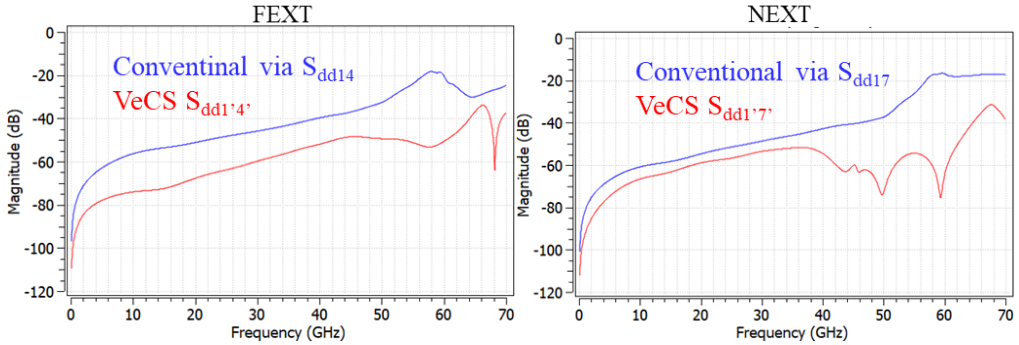
Moreover, we evaluated the crosstalk mitigation performance of the VeCS on the basis of the model shown in Fig. 7. Fig. 7 (a) shows the VeCS-based channel model, and Fig. 7 (b) represents the corresponding conventional via-based channel model for crosstalk comparison. We used four pairs of differential channels to investigate the crosstalk mitigation of the VeCS. The port settings of the S-parameter are indicated in Fig. 7.



(a) (b)

Fig. 7. 3D model of the VeCS and the conventional via for crosstalk comparison. (a) 4 pair of differential channels with VeCS, (b) 4 pair of differential channels with conventional via.

The crosstalk comparison of the VeCS and the conventional via is plotted in Fig. 8: the far-end crosstalk (FEXT) of S_{dd14} and $S_{dd1'4'}$ is plotted in Fig. 8 (a), and the FEXT of S_{dd17} and $S_{dd1'7'}$ is plotted in Fig. 8 (b). As shown in Fig. 7, S_{dd14} or $S_{dd1'4'}$ is the FEXT of two channels in different rows, and is shielded by one row GND vias, whereas S_{dd17} or $S_{dd1'7'}$ is the FEXT of two channels in the same row. From the comparison, the crosstalk on the VeCS model is far less than that on the conventional via model, by approximately 20 dB, because the crosstalk is greatly shielded by the ovel-shaped racket of the VeCS, as compared with conventional GND via shielding. The $S_{dd1'4'}$ is less than the S_{dd14} by at least 10 dB up to 60 GHz, while the $S_{dd1'7'}$ is less than the S_{dd17} by at least 5 dB up to 70 GHz.



(a) (b)

Fig. 8. Crosstalk comparison of the VeCS model and conventional via model: (a) FEXT of S_{dd14} and $S_{dd1'4'}$, (b) FEXT of S_{dd17} and $S_{dd1'7'}$.

Measurements

To further verify the advantages of VeCS technology, we conducted real measurements of the S-parameters of the designed PCB. The designed PCB of the high-speed channels with the VeCS or conventional via is shown in Fig. 9. The length of the strip-line on the high-speed channel was 2.5 inches. The conventional via or VeCS on the designed PCB was the

same as that in the 3D simulation model introduced above. Here, a 110 GHz VNA was used for the S-parameter measurement.

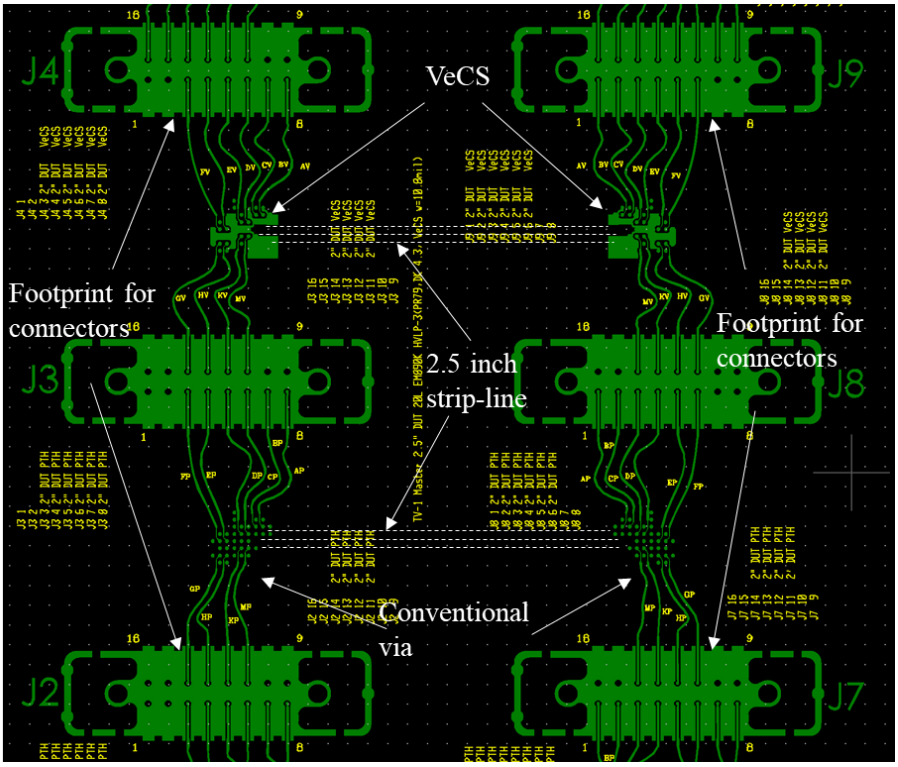
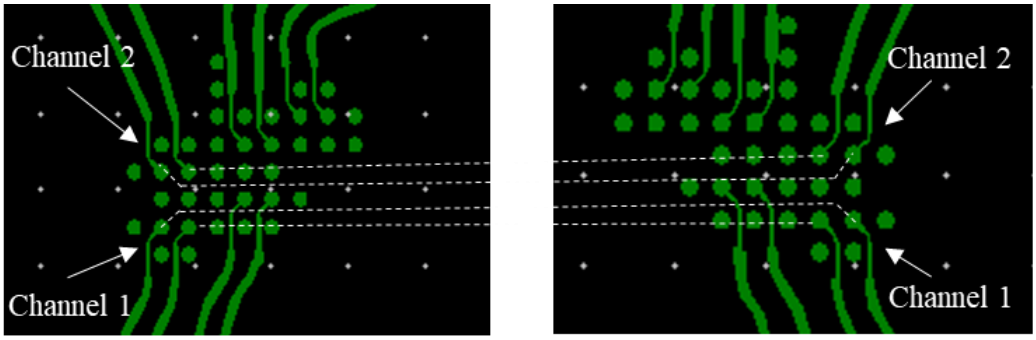


Fig. 9. Top view of the designed PCB (high-speed channels with 2.5inch strip line).

The crosstalk of channel 1 and channel 2 or channel 1´ and channel 2´ on the designed PCB is compared in Fig. 10. Fig. 10 (a) and (b) shows the layout of channel 1, channel 2, channel 1´, and channel 2´. Fig. 10 (c) shows the comparison of FEXT, and Fig. 10 (d) shows the comparison of the NEXT of the channels. As predicted by full-wave simulations, the FEXT and NEXT are greatly mitigated by VeCS technology compared with the conventional via, below a frequency of 60 GHz.



(a)

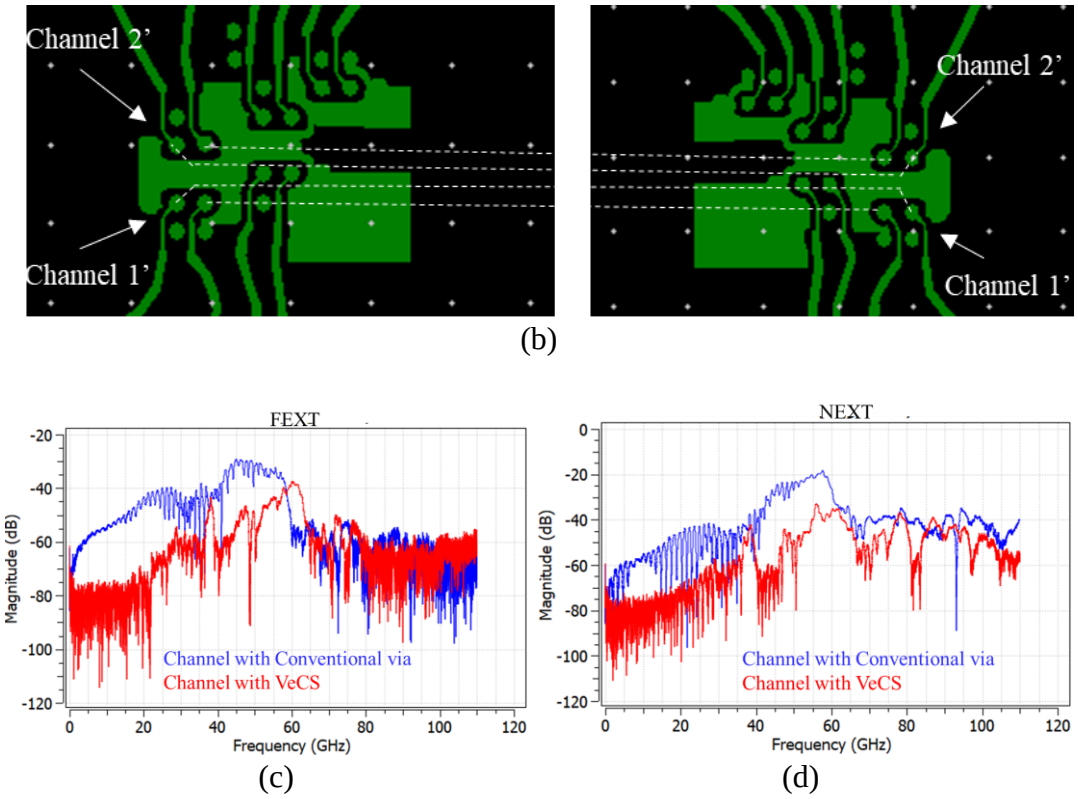
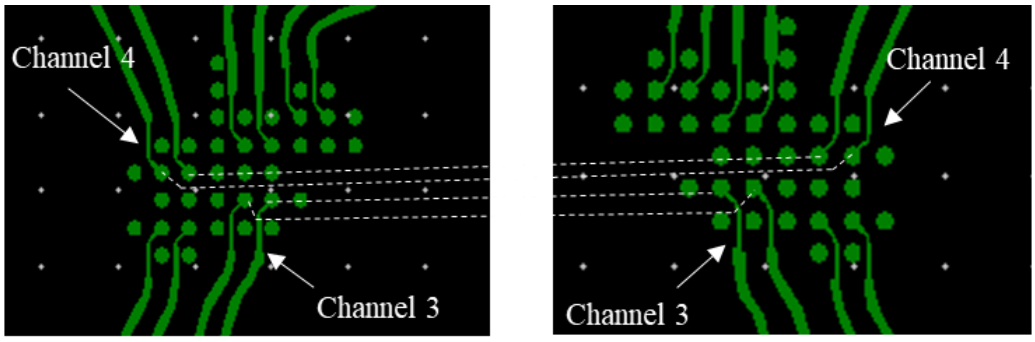


Fig. 10. Crosstalk comparison of high-speed channels on designed PCB. (a) the channel 1 and 2 with conventional vias, (b) the channel 1' and 2' with VeCS, (c) FEXT comparison, (d) NEXT comparison

Moreover, the crosstalk of channel 3 and channel 4, or channel 3´ and channel 4´, on the designed PCB is compared in Fig. 11. Fig. 11 (a) and (b) shows the layout of channel 3, channel 4, channel 3´, and channel 4´. The FEXT and NEXT of the channels are plotted in Fig. 11 (c) and (d). The FEXT and NEXT were improved by VeCS technology, as compared with the conventional via, below a frequency of 60 GHz.



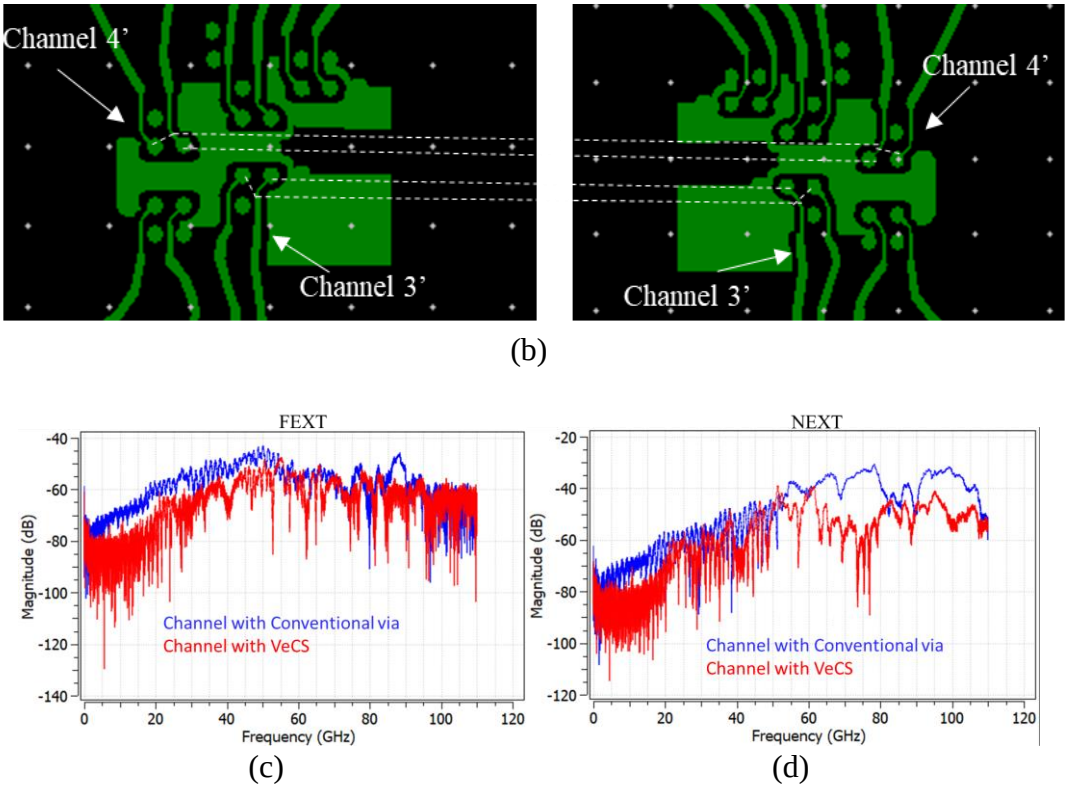


Fig. 11. Crosstalk comparison of high-speed channels on designed PCB. (a) the channel 3 and 4 with conventional vias, (b) the channel 3' and 4' with VeCS, (c) FEXT comparison, (d) NEXT comparison

Conclusion

VeCS technology was introduced and analyzed in this article. The physical structure and manufacturing processes of the VeCS were clearly presented. The electrical performance of the VeCS was subsequently analyzed and compared with conventional vias through full-wave simulations and measurements. The full-wave simulations indicated that the TDR impedance of VeCS can be easily controlled to the target impedance, in contrast to the conventional via. Thus, the return loss of the VeCS is lower than that with conventional vias. The crosstalk on the channels can be greatly mitigated by VeCS technology, particularly when the vertical signal traces of different channels are isolated by the oval-shaped racket of the VeCS. A high-speed PCB was designed to evaluate the performance of VeCS technology, wherein the crosstalk on differential channels was measured by 110 GHz VNA. The measurement results clearly showed mitigation of crosstalk by VeCS technology.

Acknowledgements

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